ABSTRACT OF THE DISCLOSURE

In a delay circuit, a semiconductor integrated circuit device containing the delay circuit, and a delay method that are excellent for adding delay times onto input signals appropriately and accurately generating delay pulses and delay signals having predetermined delay times without requiring waveform modification or delay based on parasitic elements or the like, in the buffer section of a selecting switch section, a PMOS transistor and an NMOS transistor are connected to form an output terminal. The gates are connected to an individual delayed output terminal of a delay section. The PMOS transistor is connected in series to a PMOS transistor and to a power supply voltage. In the same way, the NMOS transistor is connected in series to an NMOS transistor and to a ground potential. A control signal is input to the gate of the PMOS transistor, while an inverted signal of the control signal is input to the gate of the NMOS transistor. A selecting section is formed by the transistors.